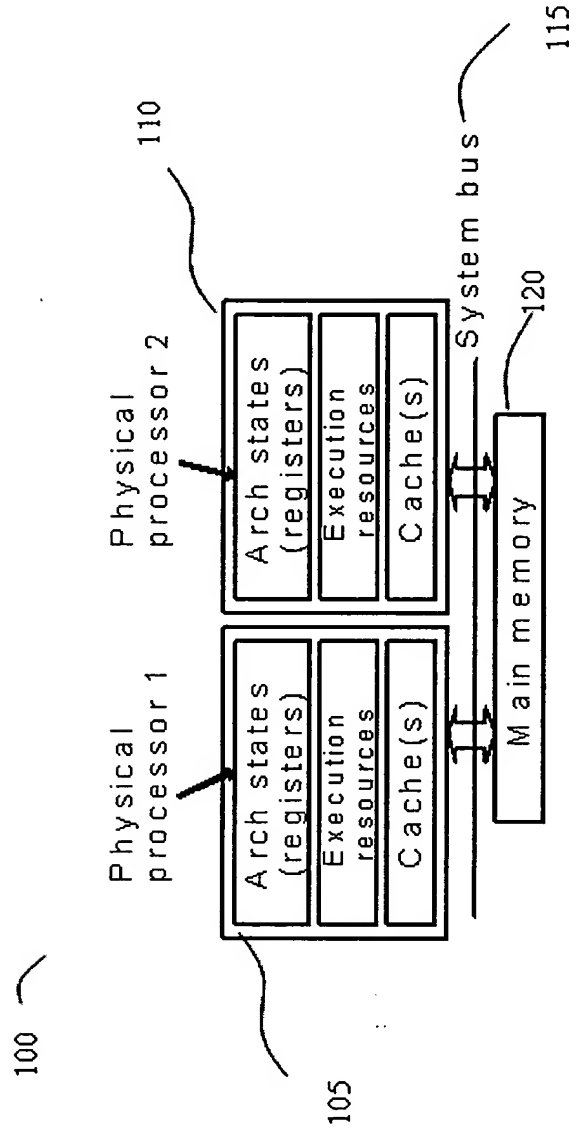


FIG. 1A (PRIOR ART)

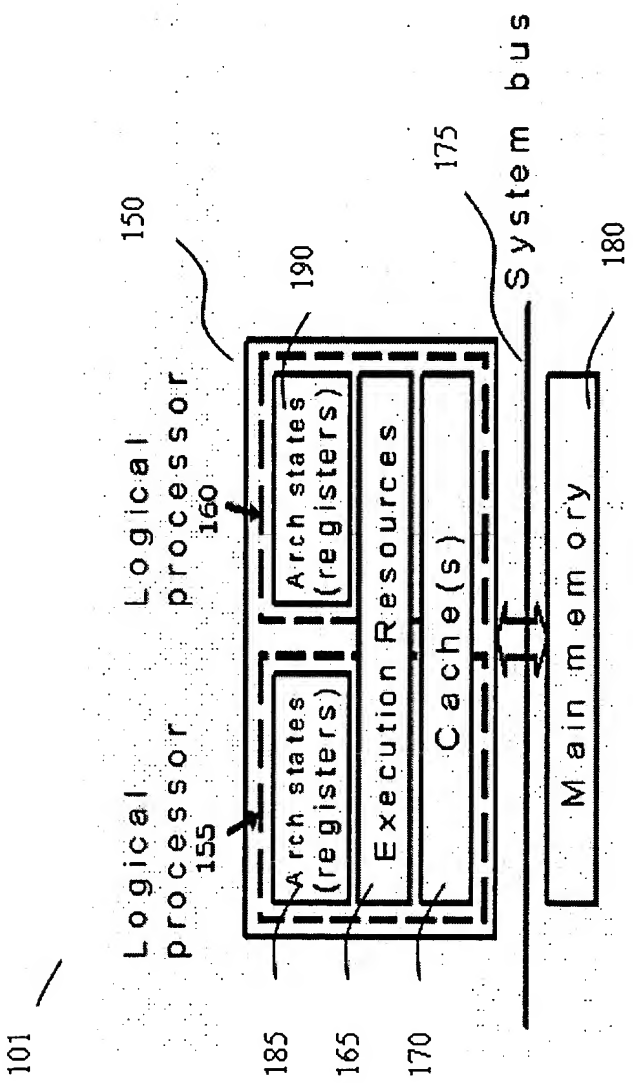

101
150
Logical processor
160
Logical processor
155
Arch states (registers)
Arch states (registers)
190
Execution Resources
Cache(s)
175
System bus
180
Main memory
185
165
170

FIG. 1B

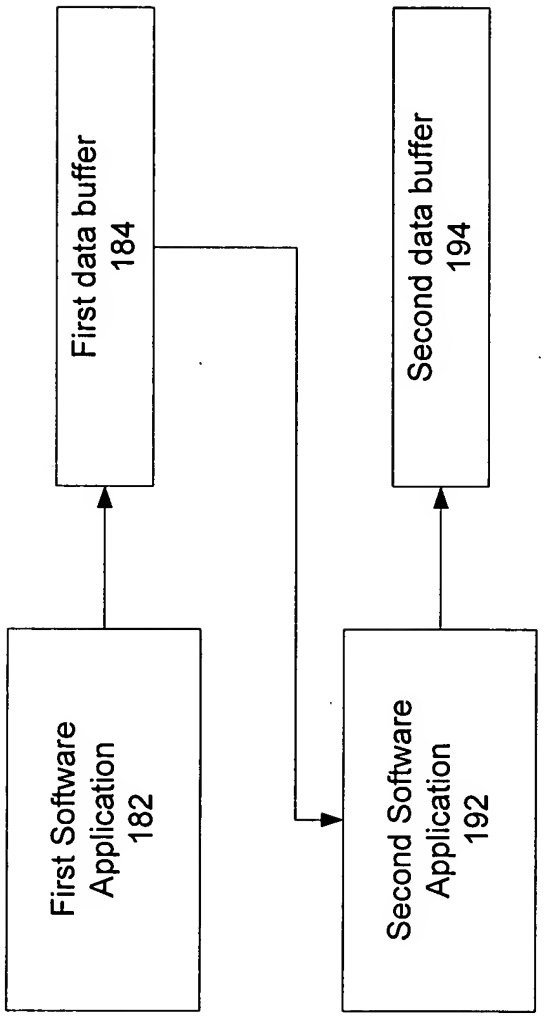

First data buffer
184
Second data buffer
194
First Software
Application
182
Second Software
Application
192

FIG. 1C

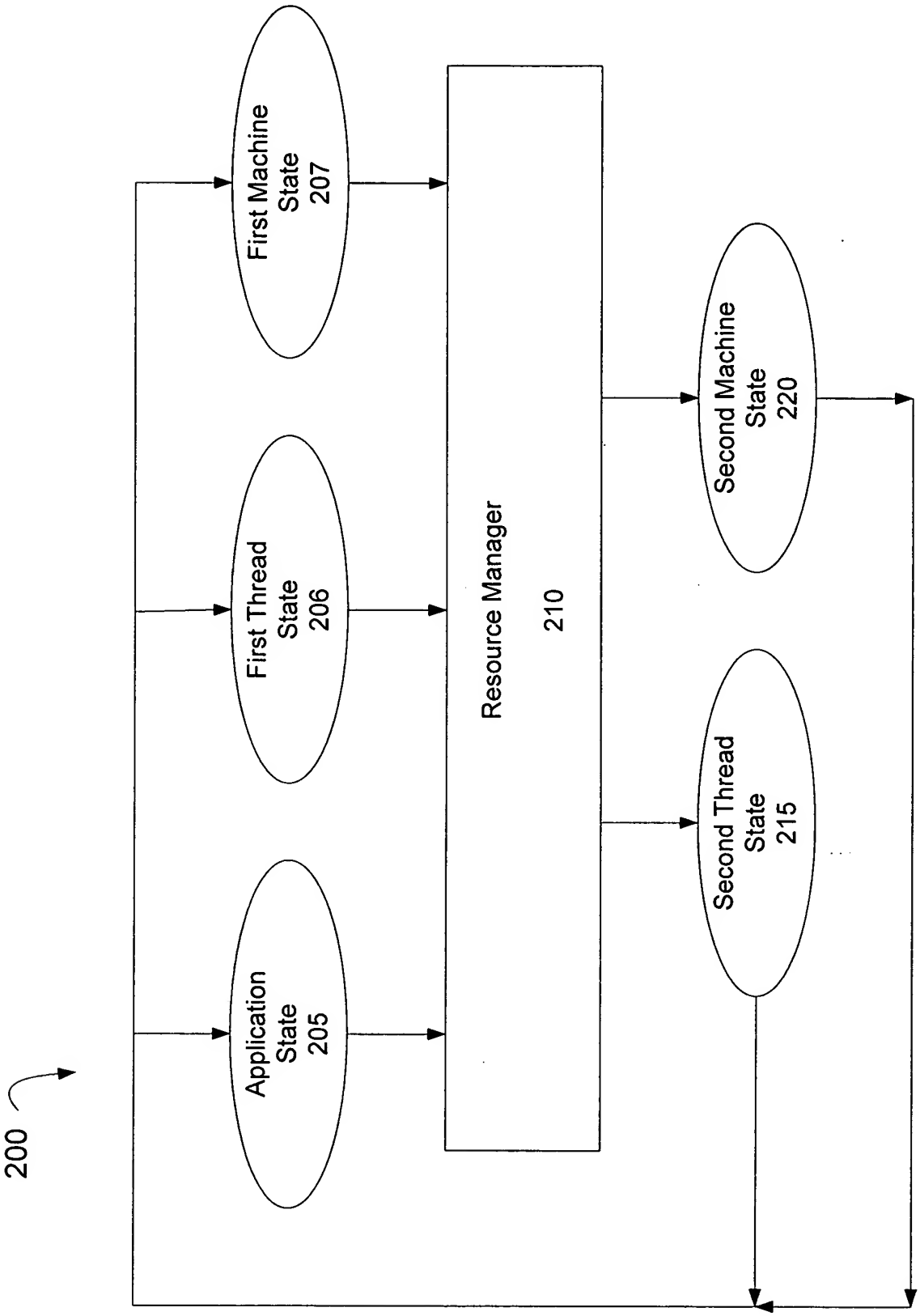

200
Application State 205
First Thread State 206
First Machine State 207
Resource Manager 210
Second Thread State 215
Second Machine State 220

FIG. 2

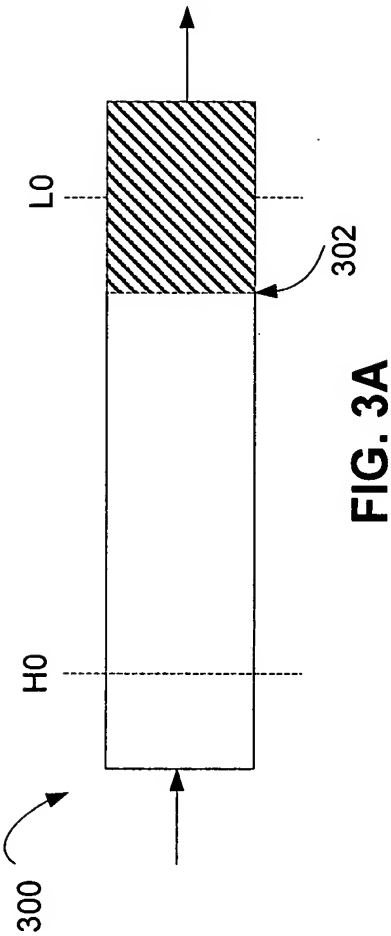

L0
302
H0
300

FIG. 3A

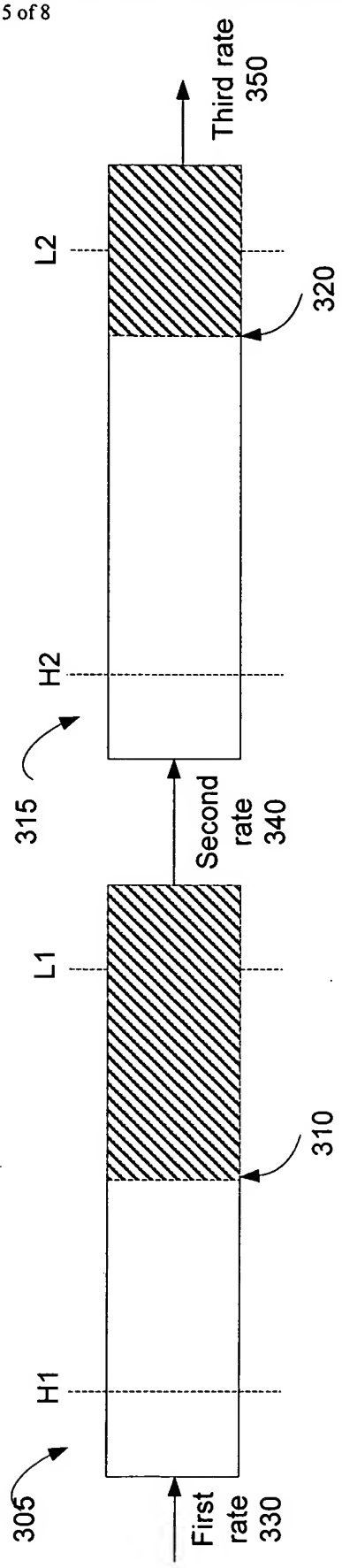

Third rate
350
L2
320
H2
315
Second rate
340
L1
310
H1
305
First rate
330

FIG. 3B

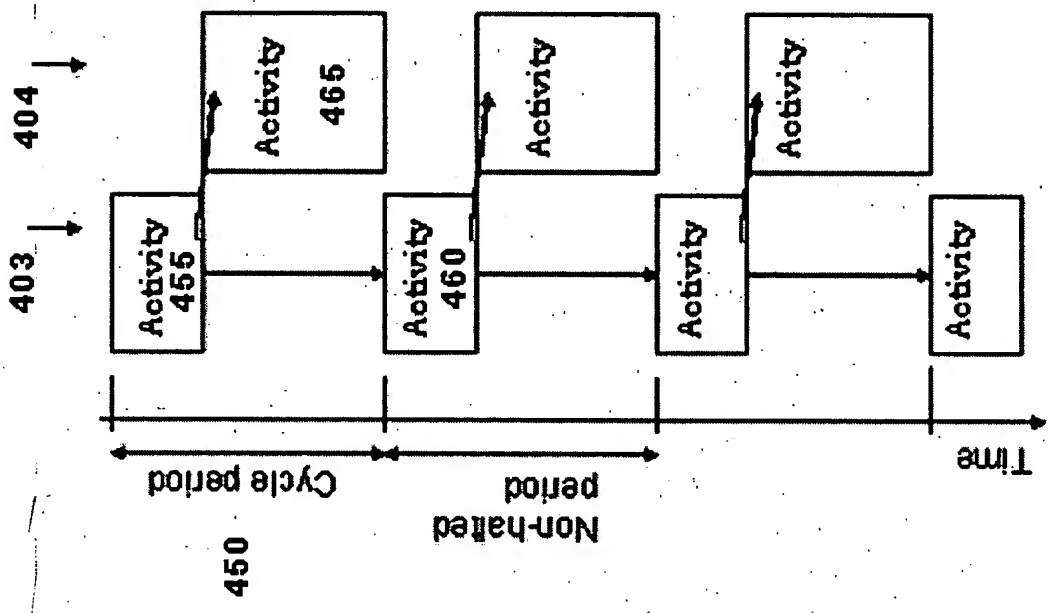

404
403
Activity 455
Activity 460
Activity
Activity 465
Time
Cycle period
Non-halted period
450

FIG. 4B

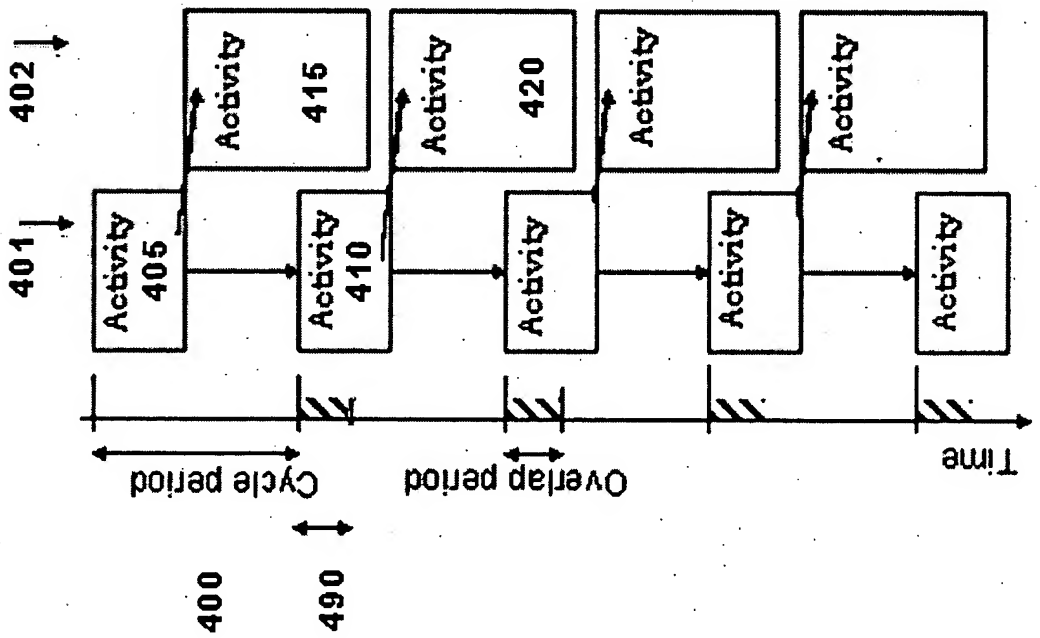
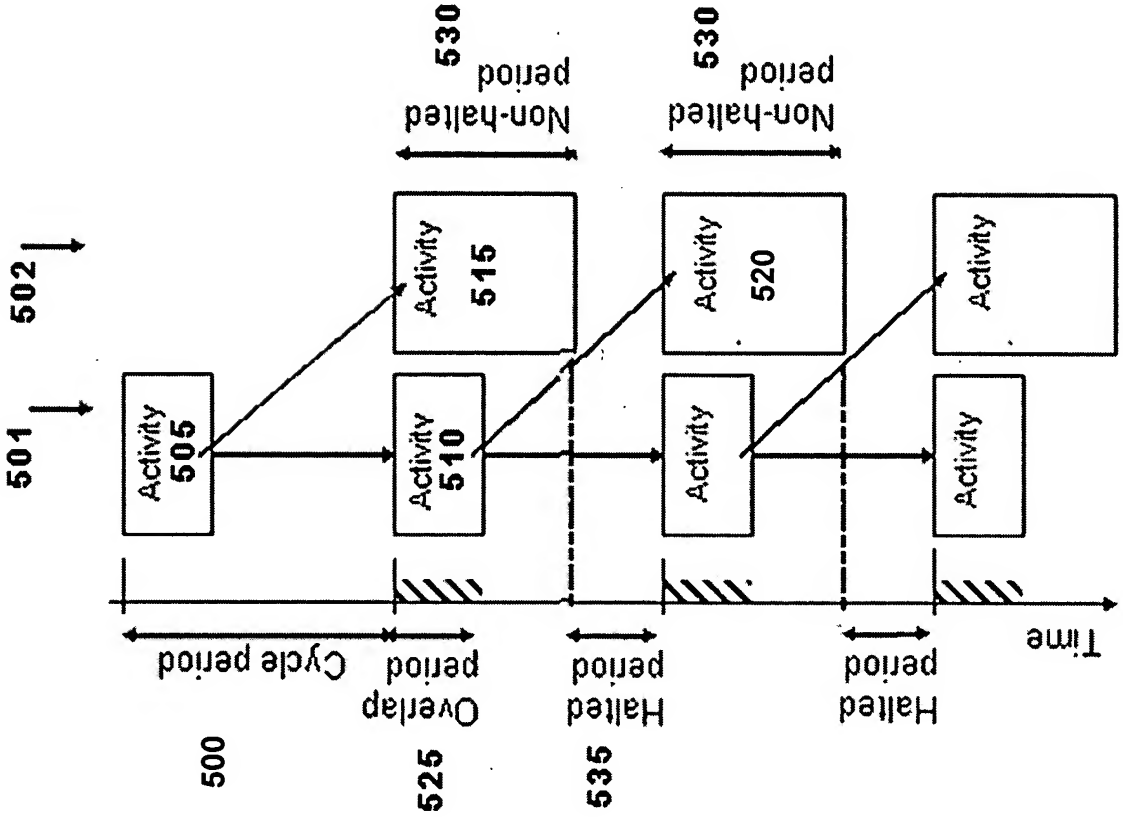

402
401
Activity 405
Activity 410
Activity 415
Activity 420
Activity
Time
Cycle period
Overlap period
400
490

FIG. 4A

FIG. 5


530
Non-halted period
530
Non-halted period
502
501
Activity 505
Activity 510
Activity 515
Activity 520
Activity
Activity
Activity
Time
Cycle period
Overlap period
Halted period
Halted period
500
525
535

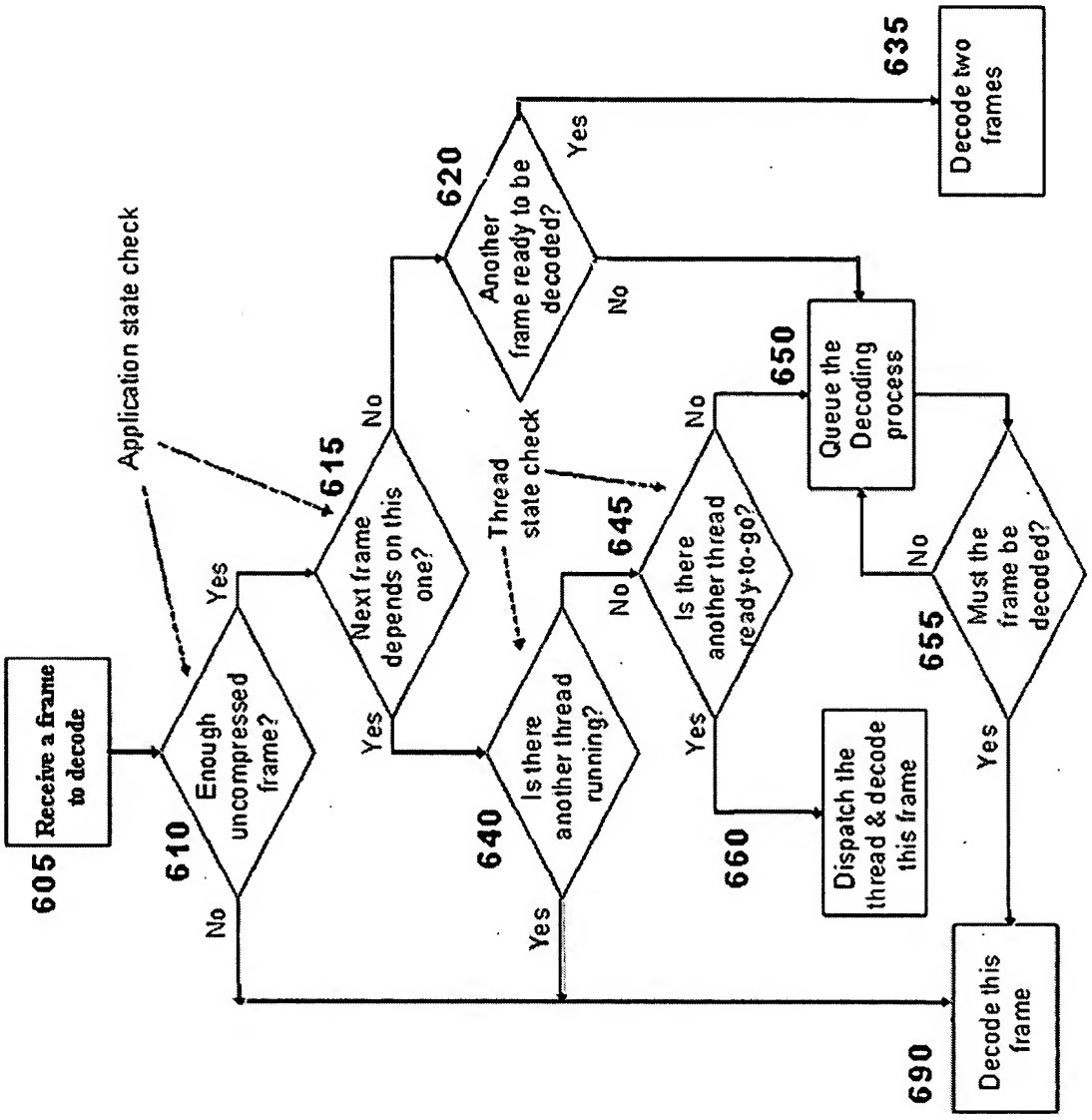

605
Receive a frame to decode
610
Enough uncompressed frame?
No
Yes
615
Next frame depends on this one?
No
Yes
620
Another frame ready to be decoded?
Yes
No
635
Decode two frames
640
Is there another thread running?
No
Yes
645
Is there another thread ready-to-go?
No
Yes
650
Queue the Decoding process
655
Must the frame be decoded?
No
Yes
660
Dispatch the thread & decode this frame
690
Decode this frame
Application state check
Thread state check

FIG. 6